REMARKS

Claims 1-3, 5-19, 21-31 and 34-45 are pending in this application. Claims 4, 20, 32 and 33 have been canceled. Claims 1, 16 and 31 have been amended to incorporate the limitations of canceled claims 4, 20, 32 and 33.

Claims 1, 2, 6, 15-17, 21, 30-31, 36 and 45 stand rejected under 35 U.S.C. § 102(e) as being anticipated by Wang et al. (U.S. Patent No. 6,376,309) ("Wang"). This rejection is respectfully traversed.

The present invention relates to a method of forming a flash memory cell utilizing atomic oxidation for fabrication of a second or top oxide layer in an oxide-nitride-oxide insulating structure. As such, amended independent claim 1 recites a "method of forming a flash memory cell" by "forming a first conductor layer over" a tunnel oxide and "forming an insulating layer over said first conductor layer." Amended independent claim 1 further recites that the insulating layer comprises "a first oxide layer over said first conductor layer, a nitride layer over said first oxide layer, and a second oxide layer over said nitride layer . . . formed by oxidizing said nitride layer with an ambient containing atomic oxygen for about 1 second to about 10 minutes."

Amended independent claim 16 recites a "method of forming an ONO insulating structure" by "depositing a first oxide layer over an integrated circuit structure; depositing a nitride layer over said first oxide layer; and growing a second oxide layer over said nitride layer . . . by oxidizing said nitride layer in the presence of atomic oxygen, and wherein said second oxide layer is formed to at least 60% of a targeted thickness of said second oxide layer."

Amended independent claim 31 recites a "method of forming a flash memory array containing a plurality of flash memory cells" by "forming a tunnel oxide on a substrate; forming a first conductor layer over said tunnel oxide" and "forming an insulating layer over said first conductor layer." Amended independent claim 31 further

recites that the insulating layer comprises "a first oxide layer over said first conductor layer, a nitride layer over said first oxide layer, and a second oxide layer over said nitride layer . . . formed by oxidizing said nitride layer in the presence of atomic oxygen at a temperature of less than about 900°C."

Wang relates to "a method of reducing the gate aspect ratio of a flash memory device." (Abstract). Wang teaches that the method includes "forming a tunnel oxide layer on a substrate; forming a polysilicon layer (406) on the tunnel oxide layer" and "forming an insulating layer (410) on the polysilicon layer." (Col. 1, lines 51-54). According to Wang, the insulating layer 410 "is a dielectric layer comprised of two oxide layers with a layer of nitride sandwiched in-between, called an ONO layer." (Col. 3, lines 41-44). Wang further teaches that "[T]he second of the two oxide layers of the dielectric layer 410 is formed using a nitride oxidation technique of about 950°C, with about 5 liters of O_2 and 9 liters of H_2 for about 40 minutes, which grows approximately 50Å of oxide." (Col. 3, lines 49-53).

Wang does not disclose all limitations of claims 1, 2, 6, 15-17, 21, 30-31, 36 and 45. Wang does not disclose forming "a first oxide layer over said first conductor layer, a nitride layer over said first oxide layer, and a second oxide layer over said nitride layer . . . formed by oxidizing said nitride layer with an ambient containing atomic oxygen for about 1 second to about 10 minutes," as amended independent claim 1 recites. Wang specifically teaches that the "second of the two oxide layers of the dielectric layer 410," which would arguably correspond to the second oxide layer of the claimed invention, is grown "for about 40 minutes," and not "for about 1 second to about 10 minutes," as amended independent claim 1 recites.

Further, Wang is silent about a "method of forming an ONO insulating structure" by "depositing a first oxide layer over an integrated circuit structure; depositing a nitride layer over said first oxide layer; and growing a second oxide layer over said nitride layer . . . by oxidizing said nitride layer in the presence of atomic oxygen, and wherein said second oxide layer is formed to at least 60% of a targeted thickness of said second oxide

layer," as amended independent claim 16 recites. Wang is also silent about a "method of forming a flash memory array," much less about "a plurality of flash memory cells" formed *inter alia* by forming "a first oxide layer over said first conductor layer, a nitride layer over said first oxide layer, and a second oxide layer over said nitride layer . . . by oxidizing said nitride layer in the presence of atomic oxygen at a temperature of less than about 900°C," as amended independent claim 31 recites. In fact, Wang teaches that the nitride oxidation technique takes place at "about 950°C, with about 5 liters of O_2 and 9 liters of H_2 for about 40 minutes" (col. 3, lines 49-53), and not at "less than about 900°C," as amended independent claim 31 recites. Since Wang fails to disclose all limitations of claims 1, 2, 6, 15-17, 21, 30-31, 36 and 45, the present invention is not anticipated under 35 U.S.C. § 102 and withdrawal of the rejection of these claims is respectfully requested.

Claims 3, 5, 11-14, 18, 19, 26-29, 34, 35 and 41-44 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Wang. This rejection is respectfully traversed.

Claims 3, 5, 18, 19, 34 and 35 depend on amended independent claims 1, 16 and 31, respectively, and recite that the second oxide layer is grown "at a temperature of less than about 900°C" (claims 3 and 18), "for about 1 second to about 10 minutes" (claims 4, 19 and 34) and "to at least about 60% of a targeted thickness of said second oxide layer" (claims 5 and 35). Claims 11-14, 26-29 and 41-44 depend on amended independent claims 1, 16 and 31, respectively, and recite that the second oxide layer "is formed in a single wafer system" (claims 11, 26 and 41), "in a batch furnace system" (claims 12, 27 and 42), "in a rapid thermal system" (claims 13, 28 and 43), "in a fast ramp system" (claims 14, 29 and 44) and "to a thickness of about 20 Å - 80 Å" (claims 15 and 45).

The subject matter of claims 3, 5, 11-14, 18, 19, 26-29, 34, 35 and 41-44 would not have been obvious over Wang. Indeed, the Office Action fails to establish a *prima facie* case of obviousness. First, not all claim limitations are taught or suggested by the prior art, considered alone or in combination. Wang does not disclose a method of forming "a first oxide layer over said first conductor layer, a nitride layer over said first

oxide layer, and a second oxide layer over said nitride layer . . . formed by oxidizing said nitride layer with an ambient containing atomic oxygen for about 1 second to about 10 minutes," as amended independent claim 1 recites. As noted above, Wang teaches the that the "second of the two oxide layers of the dielectric layer 410," which would arguably correspond to the second oxide layer of the claimed invention, is grown "for about 40 minutes," and not "for about 1 second to about 10 minutes," as amended independent claim 1 recites.

Wang also does not teach or suggest a "method of forming an ONO insulating structure," by "depositing a first oxide layer over an integrated circuit structure; depositing a nitride layer over said first oxide layer; and growing a second oxide layer over said nitride layer . . . by oxidizing said nitride layer in the presence of atomic oxygen, and wherein said second oxide layer is formed to at least 60% of a targeted thickness of said second oxide layer," as amended independent claim 16 recites. Wang is also silent about a "method of forming a flash memory array," much less about "a plurality of flash memory cells" formed *inter alia* by forming "a first oxide layer over said first conductor layer, a nitride layer over said first oxide layer, and a second oxide layer over said nitride layer . . . by oxidizing said nitride layer in the presence of atomic oxygen at a temperature of less than about 900°C," as amended independent claim 31 recites. For at least these reasons, the Office Action fails to establish a *prima facie* case for obviousness and withdrawal of the rejection of claims 3, 5, 11-14, 18, 19, 26-29, 34, 35 and 41-44 is respectfully requested.

Claims 7-10, 22-25 and 37-40 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Wang in view of Neely et al. (U.S. Patent No. 5,443,863) ("Neely"). This rejection is respectfully traversed.

Claims 7-10, 22-25 and 37-40 depend on amended independent claims 1, 16 and 31, respectively, and recite that the atomic oxygen "is supplied by ozone source" (claims 7, 22 and 37), by "plasma source" (claims 8, 23 and 38), by "microwave source" (claims 9, 24 and 39) and by "photoexcitation" (claims 10, 25 and 40).

Neely relates to low-temperature surface oxidation processes employing ozone decomposition products formed in a microwave discharge cavity. (Title; Abstract). According to Neely, ozone is first decomposed in a microwave discharge cavity into "ozone decomposition product stream" which are then directed "at the surface of the silicon-containing solid at a temperature under about 300°C." (Col. 3, lines 22-26).

The subject matter of claims 7-10, 22-25 and 37-40 would not have been obvious over Wang in view of Neely. Neither Wang nor Neely, whether considered alone or in combination, teaches or suggests the limitations of amended independent claims 1, 16 and 31 on which claims 7-10, 22-25 and 37-40 depend. Neither Wang nor Neely teaches or suggests a method of forming "a first oxide layer over said first conductor layer, a nitride layer over said first oxide layer, and a second oxide layer over said nitride layer . . . formed by oxidizing said nitride layer with an ambient containing atomic oxygen for about 1 second to about 10 minutes," as amended independent claim 1 recites. Further, neither Wang nor Neely teaches or suggests "growing a second oxide layer over said nitride layer . . . by oxidizing said nitride layer in the presence of atomic oxygen, and wherein said second oxide layer is formed to at least 60% of a targeted thickness of said second oxide layer," as amended independent claim 16 recites, or a "method of forming a flash memory array" by *inter alia* forming "a first oxide layer over said first conductor layer, a nitride layer over said first oxide layer, and a second oxide layer over said nitride layer . . . by oxidizing said nitride layer in the presence of atomic oxygen at a temperature of less than about 900°C," as amended independent claim 31 recites.

The references are also not combinable in view of the diverse areas involved in each reference. Wang refers to "a method of reducing the gate aspect ratio of a flash memory device." (Abstract). For this, Wang teaches that one of the two oxide layers of the ONO layer "is formed using a nitride oxidation technique of about 950°C, with about 5 liters of O_2 and 9 liters of H_2 for about 40 minutes, which grows approximately 50Å of oxide." (Col. 3, lines 49-53). Neely, on the other hand, refers to a method of forming "highly energetic excited states of atomic oxygen which can efficiently oxidize materials at a

temperature far less than that needed for purely thermal oxidation" and which are "quite moderate surface temperatures, often under 100°C." (Abstract). It is clear, therefore, that the rejection is based on picking and choosing selected portions of each reference, in an attempt to improperly use hindsight to reconstruct the invention. Accordingly, a person skilled in the art would not have been motivated to combine Wang with Neely and withdrawal of the rejection of claims 7-10, 22-25 and 37-40 is respectfully requested.

Attached is a marked-up version of the changes made to the claims by the current amendment. The attached page is captioned "**<u>Version with markings to show changes made.</u>**"

In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to withdraw the outstanding rejection of the claims and to pass this application to issue.

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Respectfully submitted,

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Version With Markings to Show Changes Made

1. (Amended) A method of forming a flash memory cell, comprising:

forming a tunnel oxide on a substrate;

forming a first conductor layer over [the] said tunnel oxide;

forming an insulating layer over [the] said first conductor layer, [the] said insulating layer comprising a first oxide layer over [the] said first conductor layer, a nitride layer over [the] said first oxide layer, and a second oxide layer over [the] said nitride layer, wherein [the] said second oxide layer is formed by oxidizing said nitride layer with an ambient containing atomic oxygen for about 1 second to about 10 minutes;

forming a second conductor layer over [the] said insulating layer;

etching at least [the] said first conductor layer, [the] said second conductor layer and [the] said insulating layer, thereby defining at least one stacked gate structure; and

forming a source region and a drain region in [the] said substrate on opposite side of said stacked gate structure, thereby forming at least one memory cell.

16. (Amended) A method of forming an ONO insulating structure, comprising:

depositing a first oxide layer over an integrated circuit structure;

depositing a nitride layer over said first oxide layer; and

growing a second oxide layer over said nitride layer wherein [the] said second oxide layer is formed by oxidizing said nitride layer in the presence of atomic oxygen, and wherein said second oxide layer is formed to at least 60% of a targeted thickness of said second oxide layer.

31. (Amended) A method of forming a flash memory array containing a plurality of flash memory cells, each of said plurality of flash memory cells being formed by the acts of:

forming a tunnel oxide on a substrate;

forming a first conductor layer over [the] <u>said</u> tunnel oxide;

forming an insulating layer over [the] <u>said</u> first conductor layer, [the] <u>said</u> insulating layer comprising a first oxide layer over [the] <u>said</u> first conductor layer, a nitride layer over [the] <u>said</u> first oxide layer, and a second oxide layer over [the] <u>said</u> nitride layer, wherein [the] <u>said</u> second oxide layer is formed by oxidizing said nitride layer in the presence of atomic oxygen <u>at a temperature of less than about 900°C</u>;

forming a second conductor layer over [the] <u>said</u> insulating layer;

etching at least [the] <u>said</u> first conductor layer, [the] <u>said</u> second conductor layer and [the] <u>said</u> insulating layer, thereby defining at least one stacked gate structure; and

forming a source region and a drain region in [the] <u>said</u> substrate, thereby forming at least one memory cell.